WHAT IS CLAIMED IS:

1. A negative resistance circuit comprising:

subtracting means to which an input signal is applied;

amplifying means for amplifying an output signal of the subtracting means;

positive feedback means for positively feeding back an output signal of the amplifying means to an input of the subtracting means;

dividing means for dividing the output signal of the amplifying mans;

negative feedback means for negatively feeding back a divided output signal of the dividing means; and

dividing ratio of the dividing means and amplification factor of the amplifying means being set to provide negative resistance between an input of the subtracting means and earth.

2. A negative resistance circuit according to claim 1 wherein the subtracting means is constituted by a collector-emitter dividing type amplifying circuit comprising of a npn transistor, and the amplifying means is constituted by an emitter earth type amplifying circuit comprising of a pnp transistor, the input signal being applied to a base of the npn transistor, a collector output thereof being connected to a base of the pnp transistor to take out it as said output signal.

3. A negative resistance circuit according to claim 1 wherein the subtracting means is constituted by a collector-emitter dividing type amplifying circuit comprising of a pnp transistor and the amplifying means is constituted by

an emitter earth type amplifying circuit comprising of a npn transistor, the input signal being applied to a base of the pnp transistor, a collector output thereof being connected to a base of the npn transistor to take out it as said output signal.

4. A negative resistance circuit according to claim 1 wherein the subtracting circuit is constituted by a collector-emitter dividing type amplifying circuit comprising of a first transistor and the amplifying means is constituted by an emitter earth type amplifying circuit comprising of a second transistor, the input signal being applied to a base of the first transistor, a collector output thereof being connected capacitively to a base of the second transistor to take out it as said output signal.

5. A negative resistance circuit according to claim 1 wherein the subtracting means is constituted by a drain-source dividing type amplifying circuit comprising of a first FET transistor and the amplifying means is constituted by a source earth type amplifying circuit comprising of a second FET transistor, the input signal being applied to a gate of the first FET transistor, an output thereof being connected to a gate of the second FET transistor to take out it as said output signal.